AMENDMENT TO THE DRAWINGS

Attached as an Appendix hereto are five (5) replacement sheets for figures 1-2 and 4-6, without any markings. The changes to the drawings are explained below, in the "REMARKS" section. All of the drawings on the replacement sheet, as originally filed, are provided herein. The header of each revised drawing sheet includes the following information: (i) "Replacement Sheet", (ii) application number and (iii) date information. The Examiner is requested to provide an approval of these replacement sheets in the next Office Action.

REMARKS

Claims 1-20 are currently pending in the application. By this amendment, claims 9 and 14 are amended. The specification and drawings are also revised. The above amendments do not add new matter to the application and are fully supported by the specification. For example, claims 9 and 14 were amended to replace "a high impedance" with - -at least one bias network- -, support for these amendment is in paragraphs [0026] and [0032].

Reconsideration of the rejected claims in view of the above amendments and following remarks is respectfully requested.

Amendment to Specification

The Specification was amended to correct character reference names, as well as references to curve numbers. The above amendments do not add new matter to the application and are fully supported by the specification. For example, in paragraph [0038], "first resistor 58" was changed to - -first capacitor 58- -. For example, in paragraph [0054], "Curve #1" was changed to - -Curve #5- -; "Curve #2" was changed to - -Curve #6- -; "Curve #3" was changed to - -Curve #7- -; and "Curve #4" was changed to - -Curve #8- -.

Objection to Drawings

The drawings were objected for not showing the third nFET connected in series with the first nFET and the second nFET. Applicants traverse the objection to the Drawings by the Examiner in that the specification clearly provides the necessary guidance for one of ordinarily skilled in the art to be able to utilize such a third nFET, see, e.g., paragraphs

[0032], [0035], and [0038], and an additional drawing is not necessary to facilitate the understanding of the invention by the ordinarily skilled artisan.

Accordingly, withdrawal of the drawing objection is respectfully requested.

Moreover, Applicant's have amended Figures 1-2 and 4-6 to correct labeling of character reference elements, as well as label curves and graph X and Y coordinates. The above amendments do not add new matter to the application and are fully supported by the original specification. For example, Figures 1 and 2 were amended to correct the "source" and "drain" locations on the first nFET (character reference number 32), which corresponds to the disclosure in paragraph [0026] of the Specification. Figure 4 was amended to correct the "source" and "drain" locations on the pFET (character reference number 66), which corresponds to the disclosure in paragraph [0041] of the Specification. Figures 5 and 6 were amended to even more clearly identify the curves 108 and to label the axis in order to correspond to the disclosure in paragraphs [0048-54] of the Specification.

Accordingly, Applicants respectfully requests that the Examiner reconsider and withdraw the objection of the above-noted drawings.

Claim Rejections – 35 U.S.C. § 112 Rejection

Claims 9 and 14 were rejected under 35 U.S.C. § 112, second paragraph for the limitation of "a high impedance". This rejection is respectfully traversed.

Applicants respectfully note that such language is clear and definite and that one of ordinarily skilled in the art upon reviewing the specification and claims would readily understand the scope of claims 9 and 14. However, in order to expedite prosecution of the present application, Applicants have amended claims 9 and 14 to recite - -at least one bias

network- -. In view of the above amendment, the Examiner's rejection is moot.

Therefore, Applicants request the Examiner reconsider and withdraw the 35 U.S.C. § 112, second paragraph rejection of claims 9 and 14, and indicate that these claims are in compliance with the statute.

35 U.S.C. § 103 Rejection

Claims 1-2, 5-8, 10-13, 15-18 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen (U.S. 6,556,398) (CHEN) in view of Metz et al. (U.S. 5,400,202) ("METZ"). This rejection is respectfully traversed.

The Examiner asserts that CHEN shows all of the features except a low frequency filter. However, the Examiner asserts such a feature is shown in METZ, and it would have been obvious to modify CHEN to include the features of METZ. Applicants traverse the Examiner's assertions.

The present invention relates to power clamp for an integrated circuit. In an exemplary embodiment, a power clamp 100 is connected between a power supply rail 26 and a ground rail 28. A first nFET 32 and a second nFET 30 are connected in series with one another between the power supply rail 26 and the ground rail 28, such that the drain of the first nFET 32 is connected to the power supply rail 26, the source of the first nFET 32 is connected to the drain of the second nFET 30, and the source of the second nFET 30 is connected to the ground rail 28. A first resistor 34, and a second resistor 36 are connected in series with one another between the power supply voltage rail 26 and the ground rail 28. The gate of the first nFET 32 is connected to the output of the first resistor 34 and the input of the second resistor 36. Together, the first resistor 34 and the second resistor 36

form a bias network 42. More specifically independent claims 1, 7 and 12 recite, in part:

Applicants' claim 1 recites, in part:

> "...a bias network configured to bias a gate of a first transistor of the transistor network to a portion of a voltage value of the voltage source; and
>
> a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor of the transistor network."

Applicants' claim 7 recites, in part:

> "...a voltage divider configured to a gate of the upper nFET to a prescribed value; and
>
> a low frequency filter connected to a gate of the lower nFET and configured to filter out low frequency signals between at least one power supply rail and the gate of the lower nFET."

Applicants' claim 12 recites, in part:

> coupling an electrostatic discharge event to a gate of a lower transistor of the transistor network.

Applicants submit that CHEN does not show the above features of the claimed invention for independent claims 1, 7 and 12, as admitted by the Examiner. Further, Applicants submit that no proper combination of CHEN and METZ renders obvious the above-noted features.

CHEN discloses an ESD protection circuit 20 comprising transistors 13 and 15, and two resistors 23 and 25 forming a voltage divider 21. The ESD protection circuit 20 and an internal circuit 17 are both connected to a pad 11. Further, as admitted by the Examiner, Chen fails to disclose *a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor of the transistor network*, as

recited in claim 1, or a low frequency filter, as recited in claim 7, or coupling an electrostatic discharge event to a gate of a lower transistor of the transistor network, as recited in claim 12.

METZ discloses an ESD protection circuit comprising a transient voltage on the input/output pad 15 coupling onto the gate of a MNOS trigger FET 18 , via capacitor 40, that turns on the SCR device 10. (Col. 6, lines 42-58) METZ teaches enabling the SCR to absorb a high current pulse on the CMOS pad structures caused by an ESD event (Col. 4, lines 1-2). However, METZ does not teach or suggest a trigger network configured to communicate the occurrence of an ESD event to the gate of *a second transistor of the transistor network*, as claimed in independent claims 1, 7 and 12.

Because neither CHEN nor METZ teaches or suggests a first and second transistor in which the first transistor is coupled to a bias network and the second transistor is coupled to a trigger network, as recited in at least independent claim 1, or an upper and lower nFET in which a voltage divider is coupled to the upper nFET and a low frequency filter is coupled to the lower nFET, as recited in at least independent claim 7, or coupling an electrostatic discharge event to a gate of a lower transistor of the transistor network, as recited in claim 12, Applicants submit that no proper combination of these documents can render unpatentable the instant invention.

Moreover, Applicants respectfully disagree with the Examiner's assertions that it would have been obvious to combine the teachings of METZ with those of CHEN. CHEN discloses an ESD protection circuit having a transistor with its gate connected between an upper and lower load in series with transistor with its gate coupled to its source. In contrast, METZ discloses an ESD protection circuit in which the gate of a MNOS trigger

FET 18 is coupled between a resistor R and capacitor 40 in order to turn on the SCR device 10. Thus, Applicants submit that METZ describes an alternative arrangement for the protecting circuit of CHEN, and fails to provide any teachings or suggestion for modifying CHEN in the manner asserted by the Examiner.

Thus, Applicants submit that the art of record fails to disclose the requisite motivation or rationale for combining CHEN with METZ in the manner asserted by the Examiner.

For these reasons, Applicants respectfully submit independent claims 1, 7 and 12 (and all depending claims therewith) are allowable over any proper combination of CHEN and METZ. Withdrawal of rejections of claims 1-2, 5-8, 10-13, 15-18 and 20 is respectfully requested.

Further, Applicants submit that the art of record fails to provide any teaching or suggestion for modifying the lower transistor of CHEN according to the lower transistor of METZ, nor is there any teaching or suggestion that CHEN modified as asserted, would operate in its intended manner.

Therefore, Applicants further submit that the instant rejection is based upon the use of improper hindsight after reviewing Applicants' disclosure, and not upon any teaching found in the art of record. Thus, Applicants submit the instant rejection is improper and should be withdrawn.

Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over CHEN in view of METZ and Court Decision *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). This rejection is respectfully traversed.

The Examiner is of the opinion that CHEN and METZ disclose all the elements of claims 1 and 2, and that it would have been obvious to include a high pass filter having a time constant of one microsecond. Applicants respectfully disagree with the Examiner.

Applicants note that neither CHEN nor METZ teach or suggest the recited high pass filter, such that the art of record fails to provide the requisite motivation or rationale for modifying any proper combination of CHEN and METZ that would render claim 19 obvious. Further, Applicants submit that the art of record fails to provide any teaching or suggestion that, if modified in the manner asserted by the Examiner, CHEN would operate in its intended manner. Thus, Applicants submit that the instant rejection is improper and should be withdrawn.

Further, Applicants note that the only suggestion for including a high pass filter is found in Applicants' own disclosure, such that the instant rejection is the product of the use of impermissible hindsight after review of Applicants' disclosure, which is improper and should be withdrawn.

Accordingly, Applicants request withdrawal of the rejection of claim 19.

Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over CHEN in view of METZ, in further view of Court Decision *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8, 11 (7th Cir. 1977). This rejection is respectfully traversed.

The Examiner is of the opinion that CHEN and METZ disclose all the elements of claims 1 and 2, such that the inclusion of a third transistor is obvious. Applicants respectfully disagree with the Examiner.

Neither CHEN nor METZ teach or suggest a voltage divider for one transistor and a

trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor, as claimed in independent claim 1. (see above)

For these reasons, Applicants respectfully submit that claim 1 is allowable over CHEN and METZ or any combination thereof. Claims 3 and 4 are also allowable over CHEN and METZ at least for the reason of their dependency from allowable base claim 1. Withdrawal of the rejection of claims 3 and 4 are respectfully requested.

Applicants transverse the Examiner's assertions that according to claims 3 and 4, the third transistor is connected in exacting the same way as the first transistor. In this regard applicants' claim 3 recites *a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground*, and Applicants' claim 4 recites the bias network including *a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor and a gate of the third nFET*, such that the Examiner has mischaracterized Applicants' claims.

Moreover, Applicants submit that neither document of record teaches or suggests providing an additional transistor in series with a first and second transistor, such that the Examiner's assertions of obviousness is improper and should be withdrawn.

Accordingly, Applicants request withdrawal of the rejection of claims 3 and 4.

Claims 9 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over CHEN in view of METZ, in further view of Gelecinskyi et al. (U.S. 4,916,381) (GELECINSKYI). This rejection is respectfully traversed.

The Examiner is of the opinion that CHEN and METZ disclose all the elements of claims 7 and 12, and that GELECINSKYI meets the deficiencies of CHEN and METZ. This

rejection is respectfully traversed.

Neither CHEN nor METZ teach or suggest a voltage divider for one transistor and a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor, as claimed in independent claims 7 and 12. (see above) Further, Applicants submit that GELECINSKYI likewise fails to teach the above-noted deficiencies of CHEN and METZ, such that no proper combination of these documents can render unpatentable the instant invention.

For these reasons, Applicants respectfully submit that claims 7 and 12 are allowable over any proper combination of CHEN, METZ and GELECINSKYI, and claims 9 and 14 are likewise also allowable over CHEN, METZ and GELECINSKYI at least for the reason of their respective dependency from allowable base claims 7 and 12. Therefore, withdrawal of the rejection of claims 9 and 14 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that none of the references of record, either taken alone or in any proper combination thereof,, anticipate or render obvious Applicant's invention, as recited in each of claims 1-20. The applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

Further, any amendments to the claims which have been made in this response and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed to be appropriate.

Should the Examiner have any questions or comments, he is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
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